REMARKS

Claims 16-36 are pending in this application, with claims 16, 22, and 28 being independent. Claims 37-45 have been canceled, and claims 16, 22, 28, and 36 have been amended. Support for the claim amendments may be found in the application on page 13 and in Figs. 4A-D. No new matter has been added.

The specification of the application has been objected to for various informalities. In particular, the Examiner pointed out that the "silicon oxide film" and the "gate electrodes" on page 12, lines 12-16 of the specification are designated by the same reference number "407." This typographical error was corrected in the preliminary amendment filed with the application on July 22, 2003. In that amendment, the reference number for the "silicon oxide film" was changed to "406," in accordance with Fig. 4B. Applicants, therefore, request reconsideration and withdrawal of this objection.

Independent claim 37, along with its dependent claims 38-45, have been rejected as being duplicative of claims 28-36. Applicants have canceled claims 37-45 to obviate this rejection and, consequently, request reconsideration and withdrawal of this rejection.

Independent claims 16 and 22, along with their dependent claims 17, 19, 23, and 25, have been rejected as being anticipated by Matsumoto (U.S. Patent No. 5,396,084). Applicants have amended claims 16 and 22 to obviate this rejection.

Claims 16 and 22, as amended, each recite a method of forming an active matrix circuit that includes "forming an interlayer insulating film comprising a silicon nitride layer and a silicon oxide layer over said semiconductor layer by plasma CVD, said *silicon nitride layer and said silicon oxide layer formed over said gate electrode* and said semiconductor layer" (emphasis added). Applicants request reconsideration and withdrawal of the rejection of claims 16 and 22, and their dependent claims, because Matsumoto does not describe or suggest forming an active matrix circuit by forming an interlayer insulating film that includes a silicon nitride layer and a silicon oxide layer over the recited gate electrode.

Rather, Matsumoto describes a method for forming a thin film transistor device having a driving (peripheral) circuit and a matrix circuit. Matsumoto describes forming an NMOS thin

film transistor 2 in the matrix circuit[1] of the device by, in part, forming a second interlayer insulating film 21 over a gate electrode 20 that is, in turn, formed over a first interlayer insulating film 19 (which, interestingly, acts as a gate insulating film in the matrix circuit of the device and as an interlayer insulating film in the peripheral circuit of the device). See Fig. 2, col. 5, lines 4-10; 21-27. The second interlayer insulating film 21 that is formed over the gate electrode 20, however, does not include both a silicon nitride layer and a silicon oxide layer, as claimed. Rather, the second interlayer insulating film 21 is either a silicon oxide layer or a silicon nitride layer, but not both. See col. 5, lines 8-10.

For at least this reason, applicants request reconsideration and withdrawal of the rejection of claims 16 and 22 and their dependent claims 17, 19, 23, and 25.

Claims 18, 20, 21, 24, 26 and 27, which depend from claims 16 and 22, have been rejected as being unpatentable over Matsumoto in view of Shannon (U.S. Patent No. 5,466,617). Shannon does not remedy the failure of Matsumoto to describe or suggest forming an active matrix circuit by forming an interlayer insulating film that includes a silicon nitride layer and a silicon oxide layer over the recited gate electrode. Accordingly, for at least the reasons described above, applicants request reconsideration and withdrawal of the rejection of claims 18, 20, 21, 24, 26 and 27.

Independent claim 28, and its dependent claims 29, 30, 31, and 33-36, have been rejected as being unpatentable over Matsumoto in view of Iwanaga (U.S. Patent No. 5,932,484). Applicants have amended claim 28 to obviate this rejection.

Claims 28, as amended, recites a method of forming an active matrix circuit that includes "forming an interlayer insulating film comprising a silicon nitride layer and a silicon oxide layer over said semiconductor layer by plasma CVD, said *silicon nitride layer and said silicon oxide layer formed over said gate electrode* and said semiconductor layer" (emphasis added). For at least the reasons described above, Matsumoto does not describe or suggest forming an active

[1] Notably, Matsumoto's NMOS thin film transistor 4 is used for the peripheral circuit of the device and, therefore, is not used for the active matrix circuit of the device. Accordingly, its structure is irrelevant as to claims 16, 22, and 28, which each claim a method for forming an *active matrix circuit*. ("An NMOS thin film transistor 4 *for a peripheral circuit* and an NMOS thin film transistor 2 *for a matrix circuit* ..." (emphasis added); Matsumoto, col. 3, lines 4-6).

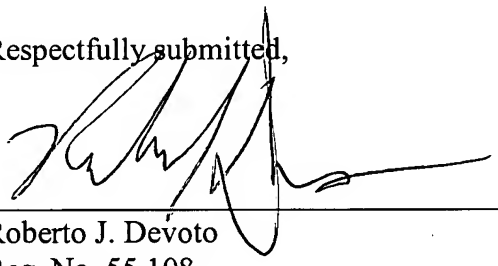
matrix circuit by forming an interlayer insulating film that includes a silicon nitride layer and a silicon oxide layer over the recited gate electrode. Iwanaga does not remedy this deficiency of Matsumoto, and, accordingly, applicants request reconsideration and withdrawal of the rejection of claim 28 and its dependent claims 29, 30, 31, and 33-36.

Claim 32, which depends from claim 28, has been rejected as being unpatentable over Matsumoto in view of Iwanaga and Shannon (U.S. Patent No. 5,466,617). As previously noted, Shannon, like Iwanaga, does not remedy the deficiency of Matsumoto to describe or suggest forming an active matrix circuit by forming an interlayer insulating film that includes a silicon nitride layer and a silicon oxide layer over the recited gate electrode. Therefore, applicants request reconsideration and withdrawal of the rejection of claim 32.

Applicants submit that all claims are in condition for allowance.

Enclosed is a $120 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,



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